Part 1: Answers to Concept Questions

1. One instance when the process leaves the CPU in a round robin scheduler is when the process completes before the time quantum has expired. The scheduler send the process to the exit state where it will be terminated. A second event when the process will leave the CPU is when the time quantum has expired and the process hasn’t completed. The scheduler will send the process from the running state to the ready state. A final event when the process leaves the CPU is when an IO bound process occurs before the time quantum expires. The scheduler will send the process to the waiting state. After the IO event is complete the scheduler will send the process back to the ready state.
2. The difference between user threads and kernel threads is that user threads are supported above the kernel and are managed without kernel support through the thread API/Library. Kernel threads, on the other hand, are supported and managed directly by the OS.

Regardless of the type of relationship (many-to-one, one-to-one, many-to-many) that OS has between user and kernel threads, user threads must be mapped to an associated kernel thread which may use a lightweight process in order to run on a CPU.

1. i)

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| P1 | P2 | P3 | P4 | P5 |
| 22 | 11 | 12 | 11 | 14 |

Turnaround time = ( (22 – 0) + (33 – 9) + (45 – 12) + (56 - 13) + (70 - 17) ) / 5 = 35 seconds

ii)

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| P1 | P2 | P3 | P4 | P5 | P1 | P2 | P3 | P4 | P5 | P1 | P2 | P3 | P4 | P5 | P1 | P2 | P3 | P4 | P5 | P1 | P5 | P1 | P1 | P1 |
| 3 | 6 | 9 | 12 | 15 | 18 | 21 | 24 | 27 | 30 | 33 | 36 | 39 | 42 | 45 | 48 | 50 | 53 | 55 | 58 | 61 | 63 | 66 | 69 | 70 |

Turnaround time = (50 + 53 + 55 + 63 + 70) / 5 = 58 seconds

d. FCFS

0 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| P1  24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 | P2 | P1 | P2 | P1 | P3 | P2 | P4 | P1 | P3 | P2 | P4 | P5 | P1 | P3 | P2 |

40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| P4 | P5 | P1 | P3 | P2 | P4 | P5 | P1 | P3 | P2 | P4 | P5 | P1 | P3 | P2 | P4 |

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| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| P5 | P1 | P3 | P2 | P4 | P5 | P1 | P3 | P2 | P4 | P5 | P1 | P3 | P4 | P5 | P1 |

56 57 58 59 60 61 62 63 64 68

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| P3 | P4 | P5 | P1 | P3 | P4 | P5 | P1 | P5 |

e.

First Come First Serve will favor longer jobs heavily. This is because any short job arriving after a job that is longer will have a longer wait time.

Round Robin will discriminate against longer jobs. This is because each job is given equal bursts of CPU time so shorter jobs that can complete in that given CPU time will complete first over the longer ones.

Multilevel Feedback Queues will discriminate against longer jobs. This is because the shortest jobs will complete first when they enter the first queue while longer jobs will get pushed back into other queues as they execute.

f.

First Fit:

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Memory | 102K | 205K | 43K | 180K | 70K | 125K | 91K | 150K |
| Job |  | T1 |  |  |  |  |  |  |

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Memory | 102K | 122K | 83K | 43K | 180K | 70K | 125K | 91K | 150K |
| Job |  | T1 |  |  | T2 |  |  |  |  |

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Memory | 102K | 122K | 83K | 43K | 105K | 75K | 70K | 125K | 91K | 150K |
| Job |  | T1 |  |  | T2 |  |  |  |  |  |

Assuming T1 completed and deallocated

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Memory | 102K | 203K | 2K | 43K | 105K | 75K | 70K | 125K | 91K | 150K |
| Job | T4 | T3 |  |  | T2 |  |  |  |  |  |

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Memory | 90K | 12K | 203K | 2K | 43K | 105K | 75K | 70K | 125K | 91K | 150K |
| Job | T4 |  | T3 |  |  | T2 |  |  |  |  |  |

Best Fit:

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Memory | 102K | 205K | 43K | 180K | 70K | 125K | 91K | 150K |
| Job |  |  |  |  |  | T1 |  |  |

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Memory | 102K | 205K | 43K | 180K | 70K | 122K | 3K | 91K | 150K |
| Job |  |  |  |  |  | T1 |  |  | T2 |

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Memory | 102K | 205K | 43K | 180K | 70K | 122K | 3K | 91K | 105K | 45K |
| Job |  |  |  |  |  | T1 |  |  | T2 |  |

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Memory | 102K | 205K | 43K | 180K | 70K | 122K | 3K | 91K | 105K | 45K |
| Job |  | T3 |  |  |  | T1 |  |  | T2 |  |

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Memory | 102K | 203K | 2K | 43K | 180K | 70K | 122K | 3K | 91K | 105K | 45K |
| Job |  | T3 |  |  |  |  | T1 |  | T4 | T2 |  |

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Memory | 102K | 203K | 2K | 43K | 180K | 70K | 122K | 3K | 90K | 1K | 105K | 45K |
| Job |  | T3 |  |  |  |  | T1 |  | T4 |  | T2 |  |

Worst Fit:

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Memory | 102K | 205K | 43K | 180K | 70K | 125K | 91K | 150K |
| Job |  | T1 |  |  |  |  |  |  |

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Memory | 102K | 122K | 83K | 43K | 180K | 70K | 125K | 91K | 150K |
| Job |  | T1 |  |  | T2 |  |  |  |  |

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Memory | 102K | 122K | 83K | 43K | 105K | 75K | 70K | 125K | 91K | 150K |
| Job |  | T1 |  |  | T2 |  |  |  |  |  |

Assuming T1 completed and deallocated memory

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Memory | 102K | 203K | 2K | 43K | 105K | 75K | 70K | 125K | 91K | 150K |
| Job |  | T3 |  |  | T2 |  |  |  |  |  |

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Memory | 102K | 203K | 2K | 43K | 105K | 75K | 70K | 125K | 91K | 150K |
| Job |  | T3 |  |  | T2 |  |  |  |  | T4 |

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Memory | 102K | 203K | 2K | 43K | 105K | 75K | 70K | 125K | 91K | 90K | 60K |
| Job |  | T3 |  |  | T2 |  |  |  |  | T4 |  |